Dual 256-Position SPI Digital Potentiometer

AD5162

FEATURES

- 2-channel, 256-position
- End-to-end resistance: 2.5 kΩ, 10 kΩ, 50 kΩ, 100 kΩ
- Compact MSOP-10 (3 mm × 4.9 mm) package
- Fast settling time: t_S = 5 µs typical on power-up
- Full read/write of wiper register
- Power-on preset to midscale
- Extra package address decode pin AD0
- Computer software replaces µC in factory programming applications
- Single supply: 2.7 V to 5.5 V
- Low temperature coefficient: 35 ppm/°C
- Low power: I_{DD} = 6 µA max
- Wide operating temperature: −40°C to +125°C
- Evaluation board available

FUNCTIONAL BLOCK DIAGRAM

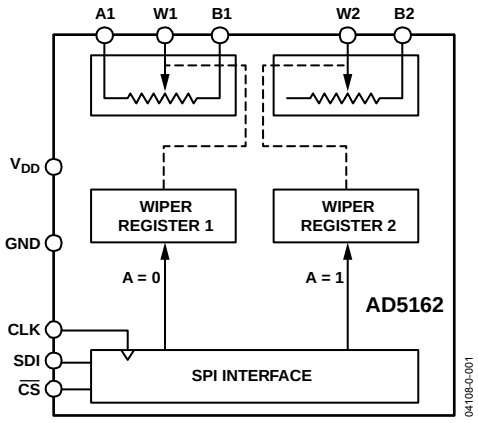

Figure 1.

APPLICATIONS

- Systems calibrations
- Electronics level settings
- Mechanical Trimmers® replacement in new designs
- Permanent factory PCB setting
- Transducer adjustment of pressure, temperature, position, chemical, and optical sensors
- RF amplifier biasing
- Automotive electronics adjustment
- Gain control and offset adjustment

GENERAL DESCRIPTION

The AD5162 provides a compact 3 mm × 4.9 mm packaged solution for dual 256-position adjustment applications. This device performs the same electronic adjustment function as a 3-terminal mechanical potentiometer. Available in four different end-to-end resistance values (2.5 kΩ, 10 kΩ, 50 kΩ, 100 kΩ), this low temperature coefficient device is ideal for high accuracy and stability variable resistance adjustments. The wiper settings are controllable through an SPI digital interface. The resistance between the wiper and either endpoint of the fixed resistor varies linearly with respect to the digital code transferred into the RDAC[1] latch.

Operating from a 2.7 V to 5.5 V power supply and consuming less than 6 µA allows the AD5162 to be used in portable battery-operated applications.

For applications that program the AD5162 at the factory, Analog Devices offers device programming software running on Windows® NT/2000/XP operating systems. This software effectively replaces any external SPI controllers, which in turn enhances users' systems time-to-market. An AD5162 evaluation kit and software are available. The kit includes a cable and instruction manual.

[1] The terms *digital potentiometer*, *VR*, and *RDAC* are used interchangeably.

Rev. A

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REVISION HISTORY

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ELECTRICAL CHARACTERISTICS—2.5 kΩ VERSION

Table 1. V_{DD} = 5 V ± 10%, or 3 V ± 10%; V_A = +V_{DD}; V_B = 0 V; −40°C < T_A < +125°C; unless otherwise noted

Parameter	Symbol	Conditions	Min	Typ[1]	Max	Unit
DC CHARACTERISTICS—RHEOSTAT MODE						
Resistor Differential Nonlinearity[2]	R-DNL	R_{WB}, V_A = no connect	−2	±0.1	+2	LSB
Resistor Integral Nonlinearity[2]	R-INL	R_{WB}, V_A = no connect	−6	±0.75	+6	LSB
Nominal Resistor Tolerance[3]	ΔR_{AB}	T_A = 25°C	−20		+55	%
Resistance Temperature Coefficient	$(\Delta R_{AB}/R_{AB})/\Delta T$	V_{AB} = V_{DD}, wiper = no connect		35		ppm/°C
R_{WB} (Wiper Resistance)	R_{WB}	Code = 0x00, V_{DD} = 5 V		160	200	Ω
DC CHARACTERISTICS—POTENTIOMETER DIVIDER MODE (Specifications Apply to All VRs)						
Differential Nonlinearity[4]	DNL		−1.5	±0.1	+1.5	LSB
Integral Nonlinearity	INL		−2	±0.6	+2	LSB
Voltage Divider Temperature Coefficient	$(\Delta V_W/V_W)/\Delta T$	Code = 0x80		15		ppm/°C
Full-Scale Error	V_{WFSE}	Code = 0xFF	−10	−2.5	0	LSB
Zero-Scale Error	V_{WZSE}	Code = 0x00	0	2	10	LSB
RESISTOR TERMINALS						
Voltage Range[5]	$V_{A, B, W}$		GND		V_{DD}	V
Capacitance[6] A, B	$C_{A, B}$	f = 1 MHz, measured to GND, Code = 0x80		45		pF
Capacitance[6] W	C_W	f = 1 MHz, measured to GND, Code = 0x80		60		pF
Common-Mode Leakage	I_{CM}	V_A = V_B = V_{DD}/2		1		nA
DIGITAL INPUTS AND OUTPUTS						
Input Logic High	V_{IH}	V_{DD} = 5 V	2.4			V
Input Logic Low	V_{IL}	V_{DD} = 5 V			0.8	V
Input Logic High	V_{IH}	V_{DD} = 3 V	2.1			V
Input Logic Low	V_{IL}	V_{DD} = 3 V			0.6	V
Input Current	I_{IL}	V_{IN} = 0 V or 5 V			±1	µA
Input Capacitance[6]	C_{IL}			5		pF
POWER SUPPLIES						
Power Supply Range	$V_{DD\ RANGE}$		2.7		5.5	V
Supply Current	I_{DD}	V_{IH} = 5 V or V_{IL} = 0 V		3.5	6	µA
Power Dissipation[7]	P_{DISS}	V_{IH} = 5 V or V_{IL} = 0 V, V_{DD} = 5 V			30	µW
Power Supply Sensitivity	PSS	V_{DD} = 5 V ± 10%, Code = midscale		±0.02	±0.08	%/%
DYNAMIC CHARACTERISTICS[8]						
Bandwidth −3 dB	BW_2.5 K	Code = 0x80		4.8		MHz
Total Harmonic Distortion	THD_W	V_A = 1 V rms, V_B = 0 V, f = 1 kHz		0.1		%
V_W Settling Time	t_S	V_A = 5 V, V_B = 0 V, ±1 LSB error band		1		µs
Resistor Noise Voltage Density	e_{N_WB}	R_{WB} = 1.25 kΩ, R_S = 0		3.2		nV/√Hz

See notes at end of section.

ELECTRICAL CHARACTERISTICS—10 kΩ, 50 kΩ, 100 kΩ VERSIONS

Table 2. V_{DD} = 5 V ± 10%, or 3 V ± 10%; $V_A = V_{DD}$; V_B = 0 V; −40°C < T_A < 125°C; unless otherwise noted

Parameter	Symbol	Conditions	Min	Typ[1]	Max	Unit
DC CHARACTERISTICS—RHEOSTAT MODE						
Resistor Differential Nonlinearity[2]	R-DNL	R_{WB}, V_A = no connect	−1	±0.1	+1	LSB
Resistor Integral Nonlinearity[2]	R-INL	R_{WB}, V_A = no connect	−2.5	±0.25	+2.5	LSB
Nominal Resistor Tolerance[3]	ΔR_{AB}	T_A = 25°C	−20		+20	%
Resistance Temperature Coefficient	$(\Delta R_{AB}/R_{AB})/\Delta T$	$V_{AB} = V_{DD}$, wiper = no connect		35		ppm/°C
R_{WB} (Wiper Resistance)	R_{WB}	Code = 0x00, V_{DD} = 5 V		160	200	Ω
DC CHARACTERISTICS—POTENTIOMETER DIVIDER MODE (Specifications Apply to All VRs)						
Differential Nonlinearity[4]	DNL		−1	±0.1	+1	LSB
Integral Nonlinearity[4]	INL		−1	±0.3	+1	LSB
Voltage Divider Temperature Coefficient	$(\Delta V_W/V_W)/\Delta T$	Code = 0x80		15		ppm/°C
Full-Scale Error	V_{WFSE}	Code = 0xFF	−2.5	−1	0	LSB
Zero-Scale Error	V_{WZSE}	Code = 0x00	0	1	2.5	LSB
RESISTOR TERMINALS						
Voltage Range[5]	$V_{A,B,W}$		GND		V_{DD}	V
Capacitance[6] A, B	$C_{A,B}$	f = 1 MHz, measured to GND, Code = 0x80		45		pF
Capacitance[6] W	C_W	f = 1 MHz, measured to GND, Code = 0x80		60		pF
Common-Mode Leakage	I_{CM}	$V_A = V_B = V_{DD}/2$		1		nA
DIGITAL INPUTS AND OUTPUTS						
Input Logic High	V_{IH}	V_{DD} = 5 V	2.4			V
Input Logic Low	V_{IL}	V_{DD} = 5 V			0.8	V
Input Logic High	V_{IH}	V_{DD} = 3 V	2.1			V
Input Logic Low	V_{IL}	V_{DD} = 3 V			0.6	V
Input Current	I_{IL}	V_{IN} = 0 V or 5 V			±1	µA
Input Capacitance	C_{IL}			5		pF
POWER SUPPLIES						
Power Supply Range	$V_{DD\ RANGE}$		2.7		5.5	V
Supply Current	I_{DD}	V_{IH} = 5 V or V_{IL} = 0 V		3.5	6	µA
Power Dissipation	P_{DISS}	V_{IH} = 5 V or V_{IL} = 0 V, V_{DD} = 5 V			30	µW
Power Supply Sensitivity	PSS	V_{DD} = 5 V ± 10%, Code = midscale		±0.02	±0.08	%/%
DYNAMIC CHARACTERISTICS						
Bandwidth −3 dB	BW	R_{AB} = 10 kΩ/50 kΩ/100 kΩ, Code = 0x80		600/100/40		kHz
Total Harmonic Distortion	THD_W	V_A = 1 V rms, V_B = 0 V, f = 1 kHz, R_{AB} = 10 kΩ		0.1		%
V_W Settling Time (10 kΩ/50 kΩ/100 kΩ)	t_S	V_A = 5 V, V_B = 0 V, ±1 LSB error band		2		µs
Resistor Noise Voltage Density	e_{N_WB}	R_{WB} = 5 kΩ, R_S = 0		9		nV/√Hz

See notes at end of section.

TIMING CHARACTERISTICS—ALL VERSIONS

Table 3. V_{DD} = +5 V ± 10%, or +3 V ± 10%; $V_A = V_{DD}$; V_B = 0 V; −40°C < T_A < +125°C; unless otherwise noted

Parameter	Symbol	Conditions	Min	Typ[1]	Max	Unit
SPI INTERFACE TIMING CHARACTERISTICS[9] (Specifications Apply to All Parts)						
Clock Frequency	f_{CLK}				25	MHz
Input Clock Pulse Width	t_{CH}, t_{CL}	Clock level high or low	20			ns
Data Setup Time	t_{DS}		5			ns
Data Hold Time	t_{DH}		5			ns
$\overline{CS}$ Setup Time	t_{CSS}		15			ns
$\overline{CS}$ High Pulse Width	t_{CSW}		40			ns
CLK Fall to $\overline{CS}$ Fall Hold Time	t_{CSH0}		0			ns
CLK Fall to $\overline{CS}$ Rise Hold Time	t_{CSH1}		0			ns
$\overline{CS}$ Rise to Clock Rise Setup	t_{CS1}		10			ns

See notes at end of section.

NOTES

[1] Typical specifications represent average readings at 25°C and V_{DD} = 5 V.
[2] Resistor position nonlinearity error R-INL is the deviation from an ideal value measured between the maximum resistance and the minimum resistance wiper positions. R-DNL measures the relative step change from ideal between successive tap positions. Parts are guaranteed monotonic.
[3] $V_{AB} = V_{DD}$, wiper (VW) = no connect.
[4] INL and DNL are measured at V_W with the RDAC configured as a potentiometer divider similar to a voltage output DAC converter. $V_A = V_{DD}$ and V_B = 0 V. DNL specification limits of ±1 LSB maximum are guaranteed monotonic operating conditions.
[5] Resistor terminals A, B, W have no limitations on polarity with respect to each other.
[6] Guaranteed by design and not subject to production test.
[7] P_{DISS} is calculated from ($I_{DD} \times V_{DD}$). CMOS logic level inputs result in minimum power dissipation.
[8] All dynamic characteristics use V_{DD} = 5 V.
[9] See timing diagrams for locations of measured values.

ABSOLUTE MAXIMUM RATINGS

Table 4. T_A = 25°C, unless otherwise noted

Parameter	Value
V_{DD} to GND	–0.3 V to +7 V
V_A, V_B, V_W to GND	V_{DD}
Terminal Current, Ax to Bx, Ax to Wx, Bx to Wx[1]	
Pulsed	±20 mA
Continuous	±5 mA
Digital Inputs and Output Voltage to GND	0 V to 7 V
Operating Temperature Range	–40°C to +125°C
Maximum Junction Temperature (T_{JMAX})	150°C
Storage Temperature	–65°C to +150°C
Lead Temperature (Soldering, 10 s)	300°C
Thermal Resistance[2] θ_{JA}: MSOP-10	230°C/W

[1] Maximum terminal current is bounded by the maximum current handling of the switches, maximum power dissipation of the package, and maximum applied voltage across any two of the A, B, and W terminals at a given resistance.

[2] Package power dissipation = (T_{JMAX} – T_A)/θ_{JA}.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

PIN CONFIGURATION

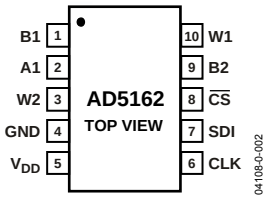

Figure 2.

PIN FUNCTION DESCRIPTIONS

Table 5.

Pin No.	Mnemonic	Description
1	B1	B1 Terminal.
2	A1	A1 Terminal.
3	W2	W2 Terminal.
4	GND	Digital Ground.
5	V_{DD}	Positive Power Supply.
6	CLK	Serial Clock Input. Positive edge triggered.
7	SDI	Serial Data Input.
8	$\overline{CS}$	Chip Select Input, Active Low. When $\overline{CS}$ returns high, data is loaded into the DAC register.
9	B2	B2 Terminal.
10	W1	W1 Terminal.

TYPICAL PERFORMANCE CHARACTERISTICS

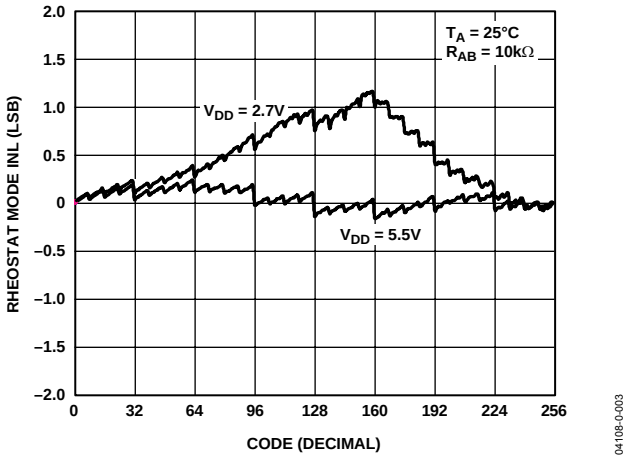

Figure 3. R-INL vs. Code vs. Supply Voltages

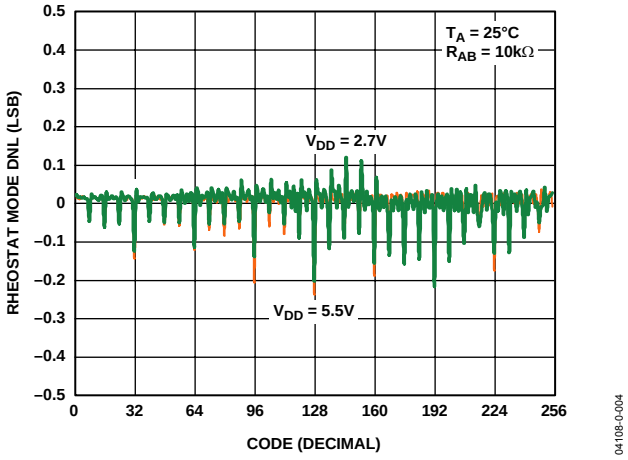

Figure 4. R-DNL vs. Code vs. Supply Voltages

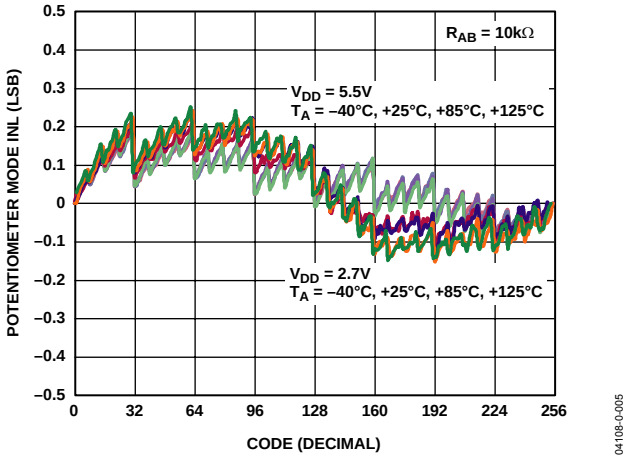

Figure 5. INL vs. Code vs. Temperature

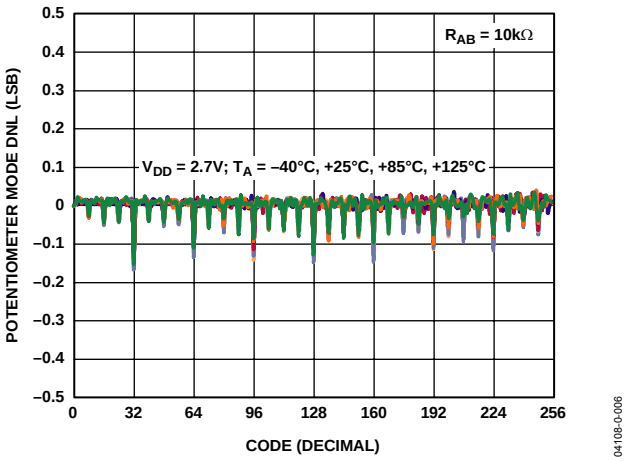

Figure 6. DNL vs. Code vs. Temperature

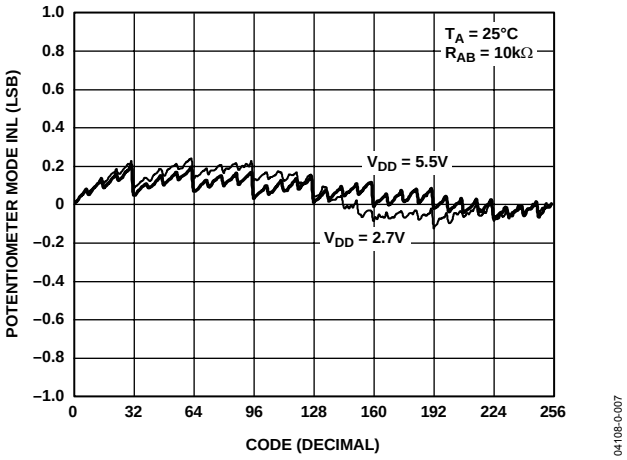

Figure 7. INL vs. Code vs. Supply Voltages

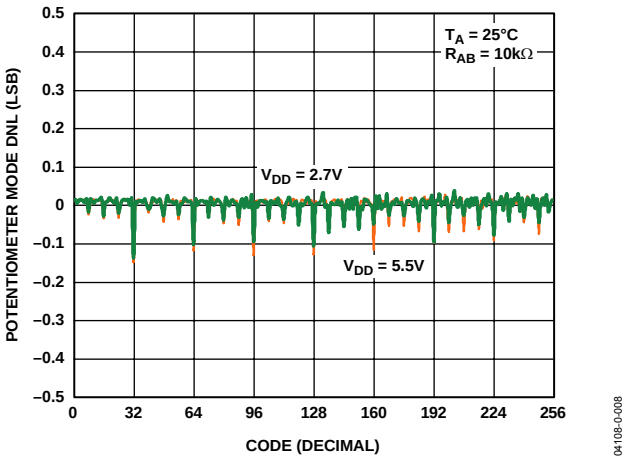

Figure 8. DNL vs. Code vs. Supply Voltages

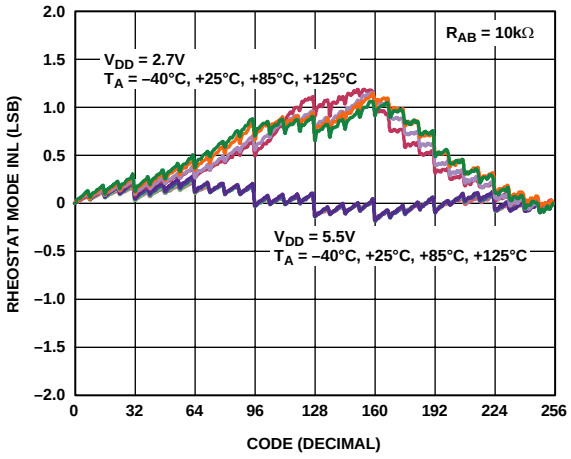

Figure 9. R-INL vs. Code vs. Temperature

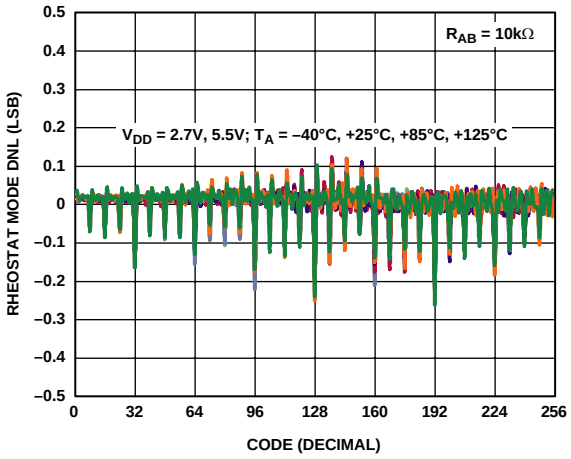

Figure 10. R-DNL vs. Code vs. Temperature

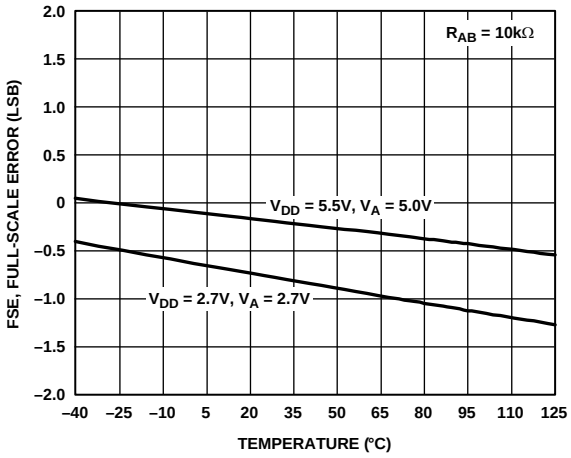

Figure 11. Full-Scale Error vs. Temperature

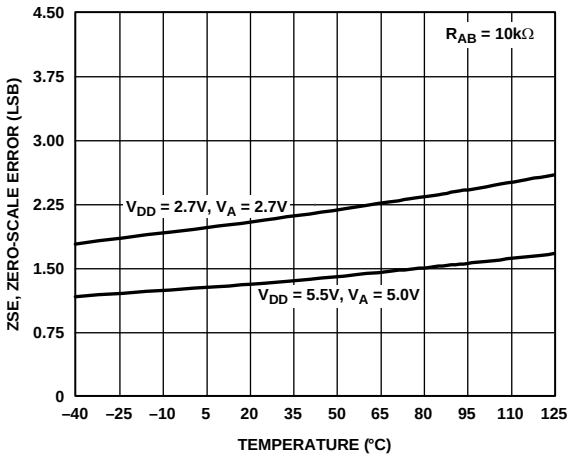

Figure 12. Zero-Scale Error vs. Temperature

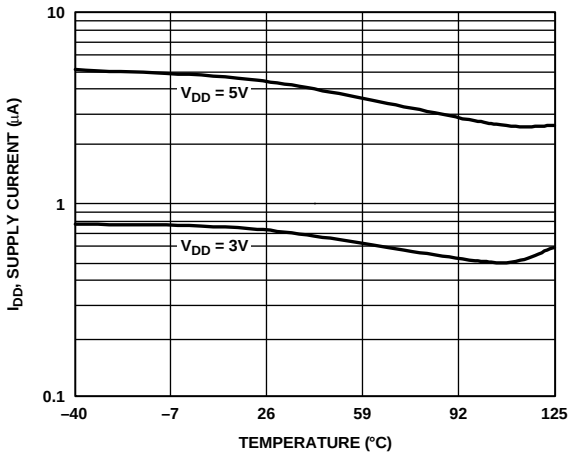

Figure 13. Supply Current vs. Temperature

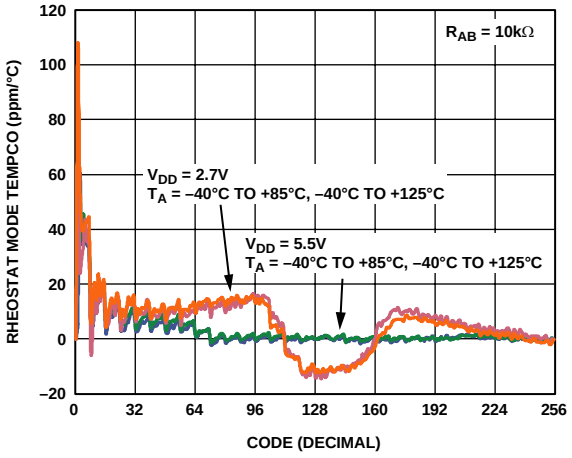

Figure 14. Rheostat Mode Tempco $\Delta R_{WB}/\Delta T$ vs. Code

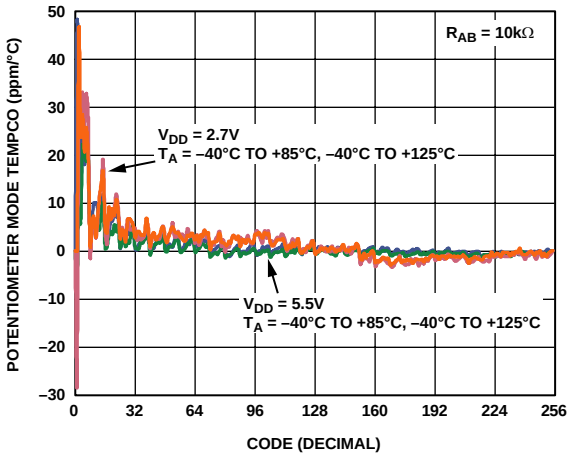

Figure 15. Potentiometer Mode Tempco $\Delta V_{WB}/\Delta T$ vs. Code

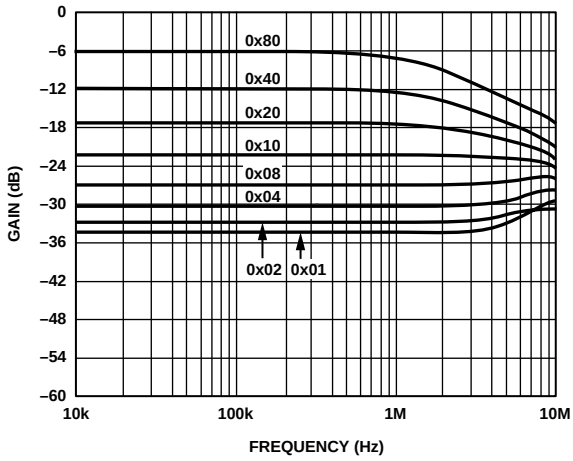

Figure 16. Gain vs. Frequency vs. Code, R_{AB} = 2.5 kΩ

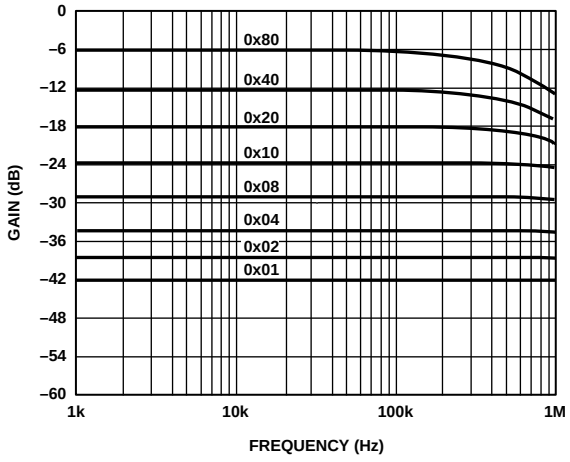

Figure 17. Gain vs. Frequency vs. Code, R_{AB} = 10 kΩ

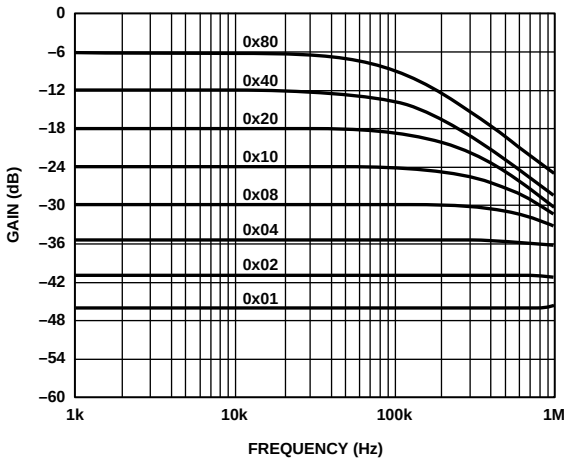

Figure 18. Gain vs. Frequency vs. Code, R_{AB} = 50 kΩ

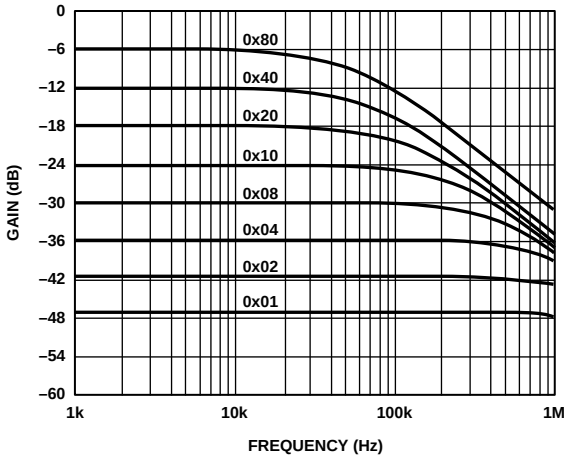

Figure 19. Gain vs. Frequency vs. Code, R_{AB} = 100 kΩ

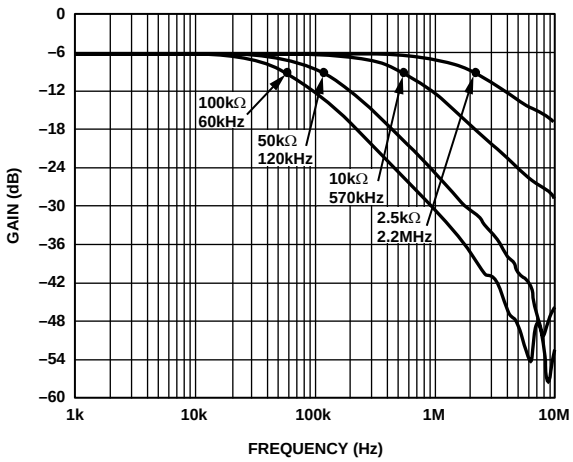

Figure 20. –3 dB Bandwidth @ Code = 0x80

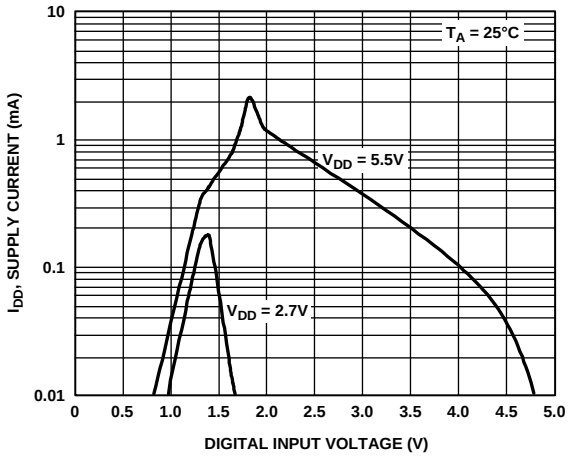

Figure 21. I_{DD} vs. Input Voltage

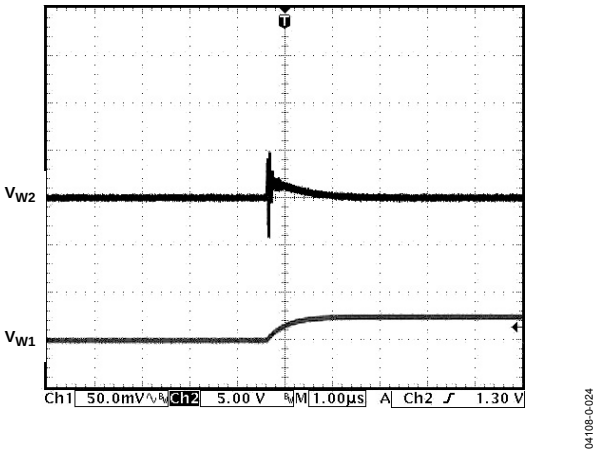

Figure 24. Analog Crosstalk

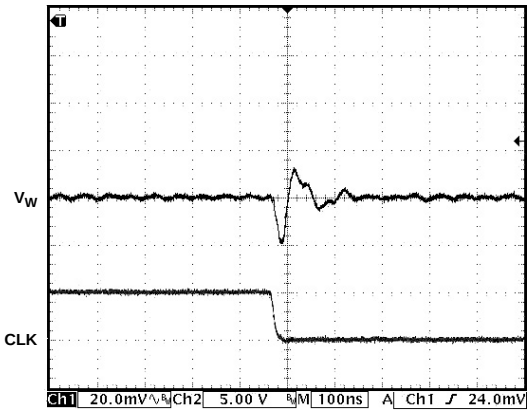

Figure 22. Digital Feedthrough

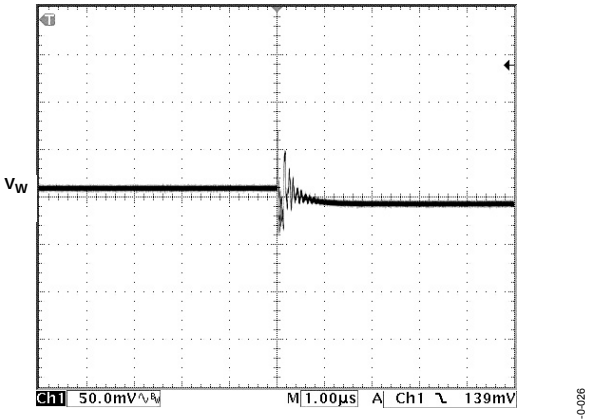

Figure 25. Midscale Glitch, Code 0x80 to 0x7F

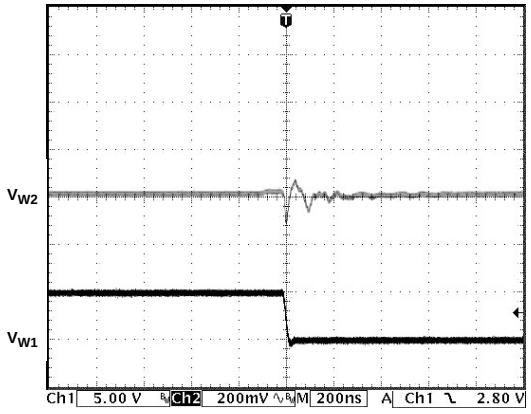

Figure 23. Digital Crosstalk

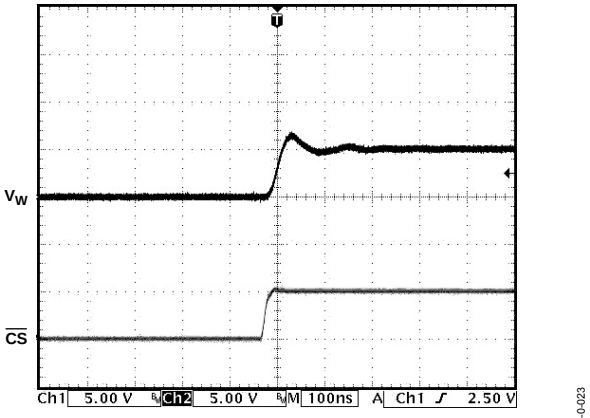

Figure 26. Large Signal Settling Time

TEST CIRCUITS

Figure 27 through Figure 32 illustrate the test circuits that define the test conditions used in the product specification tables.

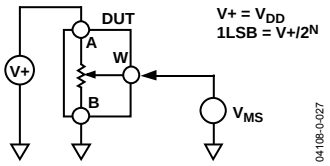

Figure 27. Test Circuit for Potentiometer Divider Nonlinearity Error (INL, DNL)

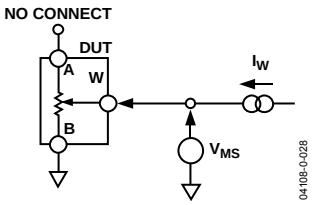

Figure 28. Test Circuit for Resistor Position Nonlinearity Error (Rheostat Operation; R-INL, R-DNL)

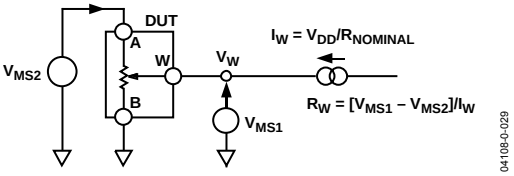

Figure 29. Test Circuit for Wiper Resistance

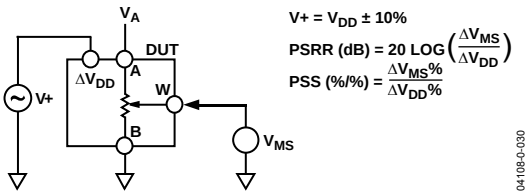

Figure 30. Test Circuit for Power Supply Sensitivity (PSS, PSSR)

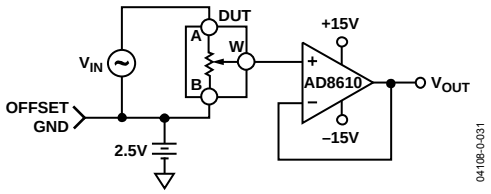

Figure 31. Test Circuit for Gain vs. Frequency

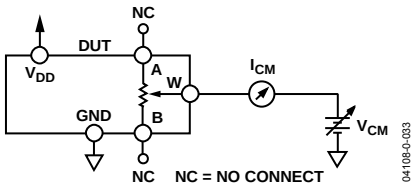

Figure 32. Test Circuit for Common-Mode Leakage Current

THEORY OF OPERATION

The AD5162 is a 256-position digitally controlled variable resistor (VR) device.

An internal power-on preset places the wiper at midscale during power-on, which simplifies the fault condition recovery at power-up.

PROGRAMMING THE VARIABLE RESISTOR AND VOLTAGE

Rheostat Operation

The nominal resistance of the RDAC between terminals A and B is available in 2.5 kΩ, 10 kΩ, 50 kΩ, and 100 kΩ. The nominal resistance (R_{AB}) of the VR has 256 contact points accessed by the wiper terminal, plus the B terminal contact. The 8-bit data in the RDAC latch is decoded to select one of the 256 possible settings.

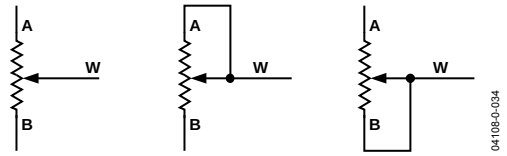

Figure 33. Rheostat Mode Configuration

Assuming that a 10 kΩ part is used, the wiper's first connection starts at the B terminal for data 0x00. Because there is a 50 Ω wiper contact resistance, such a connection yields a minimum of 100 Ω (2 × 50 Ω) resistance between terminals W and B. The second connection is the first tap point, which corresponds to 139 Ω (R_{WB} = R_{AB}/256 + 2 × R_W = 39 Ω + 2 × 50 Ω) for data 0x01. The third connection is the next tap point, representing 178 Ω (2 × 39 Ω + 2 × 50 Ω) for data 0x02, and so on. Each LSB data value increase moves the wiper up the resistor ladder until the last tap point is reached at 10,100 Ω (R_{AB} + 2 × R_W).

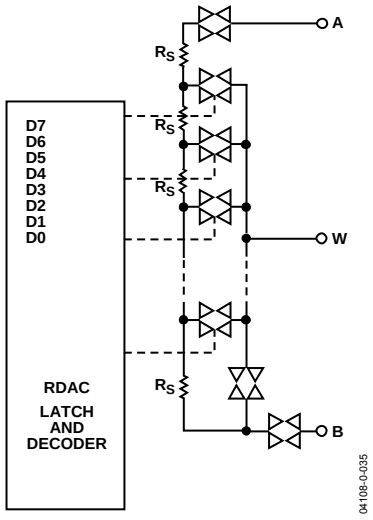

Figure 34. AD5162 Equivalent RDAC Circuit

The general equation determining the digitally programmed output resistance between W and B is

$$R_{WB}(D) = \frac{D}{256} \times R_{AB} + 2 \times R_W \quad (1)$$

where:
D is the decimal equivalent of the binary code loaded in the 8-bit RDAC register.
R_{AB} is the end-to-end resistance.
R_W is the wiper resistance contributed by the ON resistance of the internal switch.

In summary, if R_{AB} = 10 kΩ and the A terminal is open circuited, the following output resistance R_{WB} is set for the indicated RDAC latch codes.

Table 6. Codes and Corresponding R_{WB} Resistance

D (Dec)	R_{WB} (Ω)	Output State
255	9,961	Full scale (R_{AB} − 1 LSB + R_W)
128	5,060	Midscale
1	139	1 LSB
0	100	Zero scale (wiper contact resistance)

Note that, in the zero-scale condition, a finite wiper resistance of 100 Ω is present. Care should be taken to limit the current flow between W and B in this state to a maximum pulse current of no more than 20 mA. Otherwise, degradation or possible destruction of the internal switch contact can occur.

Similar to the mechanical potentiometer, the resistance of the RDAC between the wiper W and terminal A also produces a digitally controlled complementary resistance R_{WA}. When these terminals are used, the B terminal can be opened. Setting the resistance value for R_{WA} starts at a maximum value of resistance and decreases as the data loaded in the latch increases in value. The general equation for this operation is

$$R_{WA}(D) = \frac{256 - D}{256} \times R_{AB} + 2 \times R_W \quad (2)$$

For R_{AB} = 10 kΩ and the B terminal open circuited, the following output resistance R_{WA} is set for the indicated RDAC latch codes.

Table 7. Codes and Corresponding R_{WA} Resistance

D (Dec)	R_{WA} (Ω)	Output State
255	139	Full scale
128	5,060	Midscale
1	9,961	1 LSB
0	10,060	Zero scale

Typical device-to-device matching is process lot dependent and may vary by up to ±30%. Because the resistance element is processed in thin film technology, the change in R_{AB} with temperature has a very low 35 ppm/°C temperature coefficient.

PROGRAMMING THE POTENTIOMETER DIVIDER

Voltage Output Operation

The digital potentiometer easily generates a voltage divider at wiper-to-B and wiper-to-A proportional to the input voltage at A to B. Unlike the polarity of V_{DD} to GND, which must be positive, voltage across A to B, W to A, and W to B can be at either polarity.

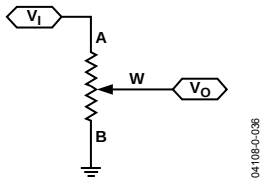

Figure 35. Potentiometer Mode Configuration

If ignoring the effect of the wiper resistance for approximation, connecting the A terminal to 5 V and the B terminal to ground produces an output voltage at the wiper-to-B starting at 0 V up to 1 LSB less than 5 V. Each LSB of voltage is equal to the voltage applied across terminal AB divided by the 256 positions of the potentiometer divider. The general equation defining the output voltage at V_W with respect to ground for any valid input voltage applied to terminals A and B is

$$V_W(D) = \frac{D}{256}V_A + \frac{256 - D}{256}V_B \quad (3)$$

A more accurate calculation, which includes the effect of wiper resistance, V_W, is

$$V_W(D) = \frac{R_{WB}(D)}{R_{AB}}V_A + \frac{R_{WA}(D)}{R_{AB}}V_B \quad (4)$$

Operation of the digital potentiometer in the divider mode results in a more accurate operation over temperature. Unlike the rheostat mode, the output voltage is dependent mainly on the ratio of the internal resistors R_{WA} and R_{WB} and not the absolute values. Therefore, the temperature drift reduces to 15 ppm/°C.

ESD PROTECTION

All digital inputs are protected with a series of input resistors and parallel Zener ESD structures shown in Figure 36 and Figure 37. This applies to the digital input pins SDI, CLK, and $\overline{CS}$.

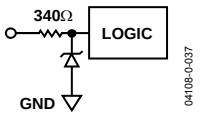

Figure 36. ESD Protection of Digital Pins

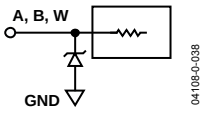

Figure 37. ESD Protection of Resistor Terminals

TERMINAL VOLTAGE OPERATING RANGE

The AD5162 V_{DD} and GND power supply defines the boundary conditions for proper 3-terminal digital potentiometer operation. Supply signals present on terminals A, B, and W that exceed V_{DD} or GND are clamped by the internal forward biased diodes (see Figure 38).

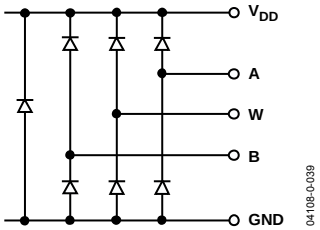

Figure 38. Maximum Terminal Voltages Set by V_{DD} and GND

POWER-UP SEQUENCE

Because the ESD protection diodes limit the voltage compliance at terminals A, B, and W (see Figure 38), it is important to power V_{DD}/GND before applying any voltage to terminals A, B, and W; otherwise, the diode is forward biased such that V_{DD} is powered unintentionally and may affect the rest of the user's circuit. The ideal power-up sequence is in the following order: GND, V_{DD}, digital inputs, and then V_A, V_B, V_W. The relative order of powering V_A, V_B, V_W, and the digital inputs is not important as long as they are powered after V_{DD}/GND.

LAYOUT AND POWER SUPPLY BYPASSING

It is good practice to employ compact, minimum lead length layout design. The leads to the inputs should be as direct as possible with a minimum conductor length. Ground paths should have low resistance and low inductance.

Similarly, it is also good practice to bypass the power supplies with quality capacitors for optimum stability. Supply leads to the device should be bypassed with disc or chip ceramic capacitors of 0.01 µF to 0.1 µF. Low ESR 1 µF to 10 µF tantalum or electrolytic capacitors should also be applied at the supplies to minimize any transient disturbance and low frequency ripple (see Figure 39). Note that the digital ground should also be joined remotely to the analog ground at one point to minimize the ground bounce.

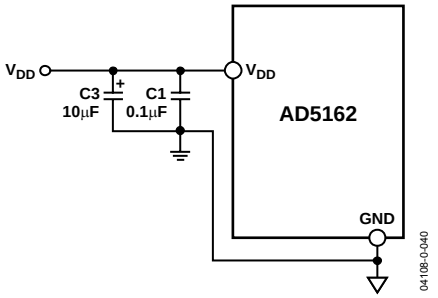

Figure 39. Power Supply Bypassing

CONSTANT BIAS TO RETAIN RESISTANCE SETTING

For users who desire nonvolatility but cannot justify the additional cost for the EEMEM, the AD5162 may be considered as a low cost alternative by maintaining a constant bias to retain the wiper setting. The AD5162 is designed specifically with low power in mind, which allows low power consumption even in battery-operated systems. The graph in Figure 40 demonstrates the power consumption from a 3.4 V 450 mAhr Li-Ion cell phone battery, which is connected to the AD5162. The measurement over time shows that the device draws approximately 1.3 µA and consumes negligible power. Over a course of 30 days, the battery is depleted by less than 2%, the majority of which is due to the intrinsic leakage current of the battery itself.

This demonstrates that constantly biasing the potentiometer is not an impractical approach. Most portable devices do not require the removal of batteries for the purpose of charging. Although the resistance setting of the AD5162 is lost when the battery needs replacement, such events occur rather infrequently such that this inconvenience is justified by the lower cost and smaller size offered by the AD5162. If and when total power is lost, the user should be provided with a means to adjust the setting accordingly.

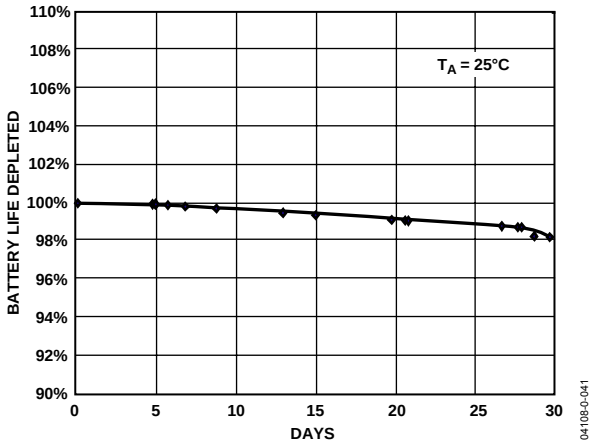

Figure 40. Battery Operating Life Depletion

EVALUATION BOARD

An evaluation board, along with all necessary software, is available to program the AD5162 from any PC running Windows 98/2000/XP. The graphical user interface, as shown in Figure 41, is straightforward and easy to use. More detailed information is available in the user manual, which comes with the board.

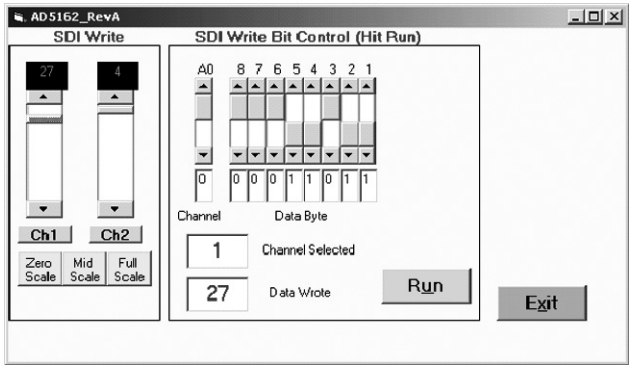

Figure 41. AD5162 Evaluation Board Software

The AD5162 starts at midscale upon power-up. To increment or decrement the resistance, the user may simply move the scrollbars on the left. To write any specific value, the user should use the bit pattern in the upper screen and press the Run button. The format of writing data to the device is shown in Table 8.

SPI INTERFACE

SPI COMPATIBLE 3-WIRE SERIAL BUS

The AD5162 contains a 3-wire SPI compatible digital interface (SDI, $\overline{CS}$, and CLK). The 9-bit serial word must be loaded MSB first. The format of the word is shown in Table 8.

The positive-edge sensitive CLK input requires clean transitions to avoid clocking incorrect data into the serial input register. Standard logic families work well. If mechanical switches are used for product evaluation, they should be debounced by a flip-flop or other suitable means. When $\overline{CS}$ is low, the clock loads data into the serial register on each positive clock edge (see Figure 42).

The data setup and data hold times in the specification table determine the valid timing requirements. The AD5162 uses a 9-bit serial input data register word that is transferred to the internal RDAC register when the $\overline{CS}$ line returns to logic high. Extra MSB bits are ignored.

Table 8. Serial Data-Word Format

B8	B7	B6	B5	B4	B3	B2	B1	B0
A0	D7	D6	D5	D4	D3	D2	D1	D0
MSB								LSB
2^8	2^7							2^0

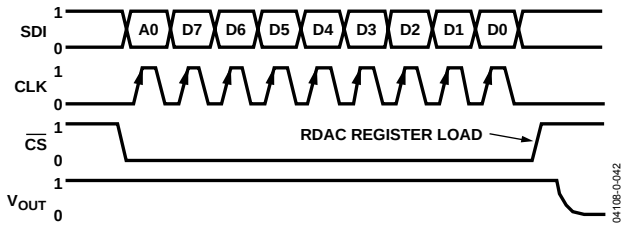

Figure 42. SPI Interface Timing Diagram (V_A = 5 V, V_B = 0 V, $V_W = V_{OUT}$)

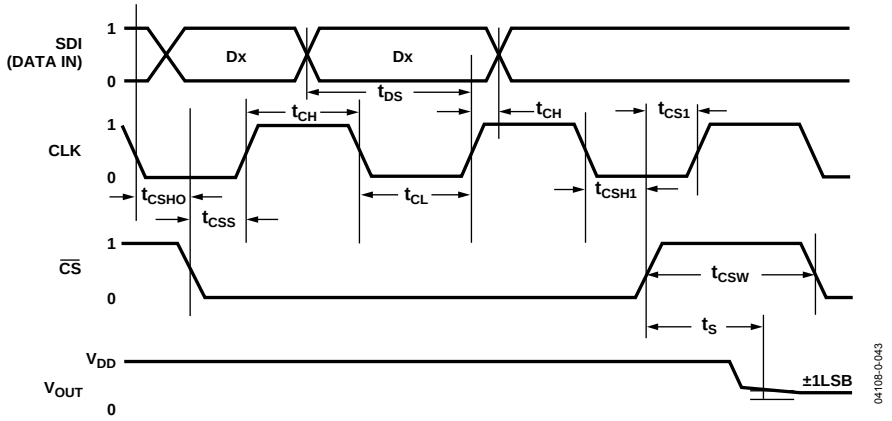

Figure 43. SPI Interface Detailed Timing Diagram (V_A = 5 V, V_B = 0 V, $V_W = V_{OUT}$)

OUTLINE DIMENSIONS

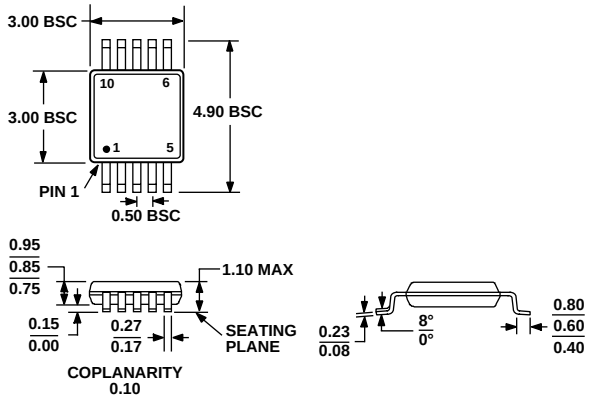

Figure 44. 10-Lead Mini Small Outline Package [MSOP]
(RM-10)
Dimensions shown in millimeters

ORDERING GUIDE

Model	R_{AB} (Ω)	Temperature	Package Description	Package Option	Branding
AD5162BRM2.5	2.5 k	–40°C to +125°C	MSOP-10	RM-10	D0Q
AD5162BRM2.5-RL7	2.5 k	–40°C to +125°C	MSOP-10	RM-10	D0Q
AD5162BRM10	10 k	–40°C to +125°C	MSOP-10	RM-10	D0R
AD5162BRM10-RL7	10 k	–40°C to +125°C	MSOP-10	RM-10	D0R
AD5162BRM50	50 k	–40°C to +125°C	MSOP-10	RM-10	D0S
AD5162BRM50-RL7	50 k	–40°C to +125°C	MSOP-10	RM-10	D0S
AD5162BRM100	100 k	–40°C to +125°C	MSOP-10	RM-10	D0T
AD5162BRM100-RL7	100 k	–40°C to +125°C	MSOP-10	RM-10	D0T
AD5162EVAL	See Note 1		Evaluation Board		

[1]The evaluation board is shipped with the 10 kΩ R_{AB} resistor option; however, the board is compatible with all available resistor value options.

NOTES

NOTES

NOTES

C04108–0–11/03(A)